IN THE CLAIMS:

Claim 1. (Currently amended) An integrated circuit test device comprising:

a substrate having an integrated circuit thereon and including interconnects formed within a ~~by an internal metallization~~ layer on said substrate;

a plurality of bond pads formed about an outer region of said substrate; and

a conductive trace formed on said ~~by said internal metallization~~ layer and coupled to at least two of said plurality of bond pads, said conductive trace and said at least two of said plurality of bond pads electrically isolated from said integrated circuit and said interconnects.

Claim 2. (Previously amended) The integrated circuit test device of Claim 1 wherein said conductive trace surrounds said plurality of bond pads.

Claim 3. (Previously amended) The integrated circuit test device of Claim 2 wherein said conductive trace has a chamfered region.

Claim 4. (Canceled)

Claim 5. (Previously amended) The integrated circuit test device of Claim 1 further comprising at least two separate conductive traces.

Claim 6. (Previously amended) The integrated circuit test device according to Claim 5 wherein said at least two separate conductive traces have a varying height relative to an upper surface of said substrate.

Claim 7. (Previously amended) The integrated circuit test device according to Claim 1 wherein said conductive trace is formed at the periphery of said integrated circuit.

Claim 8. (Previously amended) The integrated circuit test device of Claim 1 further comprising at least two separate isolated conductive traces, each of said separate isolated conductive traces coupled to at least two of said plurality of bond pads.

Claim 9. (Canceled)

Claim 10. (Currently amended) An integrated circuit test device comprising:

a substrate having an integrated circuit thereon and including interconnects formed within a ~~by an internal metallization~~ layer on said substrate;

a plurality of bond pads formed about an outer region of said substrate; and

a conductive test circuit on said ~~substrate consisting of~~ substrate, including a conductive trace formed ~~by~~ on said ~~internal metallization~~ layer and electrically coupled to at least two of said plurality of bond pads, said conductive test circuit electrically isolated from said integrated circuit and said interconnects.

Claim11. (Previously amended) The integrated circuit test device of Claim 10 further comprising a plurality of conductive traces.

Claim12. (Previously amended) The integrated circuit test device according to Claim 11 wherein at least two of said plurality of conductive traces have a varying height relative to an upper surface of said substrate.

Claim 13. (Previously amended) The integrated circuit test device of Claim 10 wherein said conductive trace has a chamfered region.

Claims 14-15 (Canceled)